



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/604,530	06/27/2000	Atsuko Kozai	KOM-02001	4994

26339 7590 12/19/2003

PATENT GROUP  
CHOATE, HALL & STEWART  
EXCHANGE PLACE, 53 STATE STREET  
BOSTON, MA 02109

EXAMINER

DIMYAN, MAGID Y

ART UNIT PAPER NUMBER

2825

DATE MAILED: 12/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

### Application No.

09/604,530

### Applicant(s)

KOZAI, ATSUKO

### Examiner

Magid Y Dimyan

### Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 03 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 4-9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 4-7 and 9 is/are rejected.
- 7) ☒ Claim(s) 8 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 June 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. §§ 119 and 120

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 10202003. 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Acknowledgement***

1. Receipt is acknowledged of the Response to Restriction Requirement, filed October 03, 2003. It is also acknowledged that the applicant has elected Group II (claims 4 – 9), drawn to a method for executing a placement and routing of standard cells, for prosecution.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eng (U.S. Patent No. 6,145,117) in view of Gheewala (U.S. Patent No. 5,923,060) and further in view of Schultz (Pub. No. US 2003/0014201). Referring to that claim, Eng discloses a standard cell placement and routing (P & R) process system comprising a library file of standard cells (see Figs. 6, 12, 13; column 15, lines 35 – 65); a constraint information file

which stores constraint information and parameters (including frequency, voltage, etc) concerning P & R (see Fig. 13, block 222; column 9, line 65 to column 10, line 29); and an input/output and display apparatus for displaying history and the result of P & R (see Fig. 14). All the limitations cited in the claim are thus disclosed by Eng except for (a) the power supply terminals on a diffusion layer; and (b) using the sheet resistance information of the diffusion layer in the P & R system for executing the P & R of standard cells. However, Gheewala teaches an array basic cell (i.e., standard cell) and circuit layout architecture for efficiently routing power supply traces by making use of diffusion regions to make the appropriate power supply connections, as claimed herein (see column 1, line 10 to column 2, line 10; Fig. 4). Furthermore, Schultz cites a floor plan development voltage drop analysis tool for analyzing power bus wire segments in a power bus grid of an IC that in fact uses the sheet resistance of the wire segments in the analysis. Since, as stated by Gheewala, using diffusion layers in the power supply connections reduces the area of basic cells (and hence increases the gate density); and furthermore, as stated by Schultz using the sheet resistance of power grid wires can more accurately analyze and map the power-bus grid in a design, it would therefore be obvious to one having ordinary skill in the art at the time the invention was made to combine all three disclosures to achieve the same invention as claimed herein.

4. Claims 5, 6, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eng in view of Gheewala, further in view of Schultz, and further in view of Nawa (U.S. Patent No. 6,405,346). The teachings of Eng, Gheewala and Schultz are cited in

(3) above, and described in detail in their disclosures. All the limitations recited in these claims pertaining to the P and R method for executing a P & R of standard cells that use power supply lines/terminals of diffused layers, are cited in (3) above, as well as by Eng, Gheewala and Schultz, except for the step of discriminating whether or not the power supply resistance is less than, or greater than, a predetermined value. However, Nawa teaches a method for optimizing power supply wiring in an IC that checks for maximum voltage drop (i.e., power supply resistance) in a power supply network and makes the appropriate corrections to the line width, etc. See Figs. 2A, 2B; 4A, 4B; column 1, lines 6 - 28. Since, as stated by Nawa, it would be very beneficial to be able to provide a method and apparatus for designing the optimal power supply wiring in complex IC designs (see column 2, lines 53 - 55), it would therefore be obvious to one having ordinary skill in the art at the time the invention was made to combine all four disclosures to obtain the same inventions as claimed herein.

### ***Allowable Subject Matter***

5. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: this claim includes the additional limitation of being able to detect a signal line

which becomes a hindrance in reducing the resistance of a power supply line, and being able to overcome this hindrance by providing appropriate through-holes in the layout of the IC. Prior art does not teach this limitation.

### ***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,446,245 to Xing et al teaches a method and apparatus for performing power routing in an ASIC design; whereby the power routing is performed after cell placement, allowing more knowledgeable placement of power structures in the physical layout.

U.S. Patent No. 5,349,542 to Brasen et al calculates segments within a power network of an IC utilizing information generated during design and placement.

U.S. Patent No. 6,069,373 to Iwaki discloses a compact semiconductor device using SOI – CMOS technology, and shows how diffusion layers can be used to be able to connect to a power source.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y Dimyan whose telephone number is (703) 308-1354. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (703) 308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Magid Y Dimyan  
Examiner  
Art Unit 2825

myd  
December 9, 2003

